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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,083	04/19/2001	Woo Sik Yoo	M-11439 US	9578

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EXAMINER	
FOX, CHARLES A	
ART UNIT	PAPER NUMBER
3652	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/838,083	Applicant(s) YOO, WOO SIK
	Examiner Charles A. Fox	Art Unit 3652

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-9,11-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-9,11-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 11-13, 18 and 19 are rejected under 35 U.S.C. 102(a) as being anticipated by Suda et al. In regards to claim 11 Suda et al. US 6,053,980 discloses a system for transporting semiconductor wafers comprising:

a process system including a process chamber (56) and a transport module (10);

a wafer transport device (20) disposed in said transport module (10);

a load lock chamber (52);

a container (40) configured to hold a plurality of wafers;

said container being and remaining a separate component from said processing system;

wherein said wafer transport device is designed to extend into said container and remove a wafer for delivery to a load lock chamber;

wherein said transport device (20) is exposed to the ambient environment outside of said processing system while extending into said container.

In regards to claim 12 Suda et al. also disclose that said wafer transport device comprises a robot with an extensible arm and an end effector.

In regards to claim 13 Suda et al. further disclose that the wafer transport device is fixed within the transport chamber.

In regards to claim 18 Suda et al. also discloses a gate valve (62) assembly between the transport module and the process chamber.

In regards to claim 19 Suda et al. disclose that the wafer container is a cassette.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda et al. in view of Gordon et al. In regards to claims 1 and 14 Suda et al. teach a method of transporting semiconductor wafers comprising the steps of:

providing a processing system including a transport module and a process chamber;

extending a transport robot into a cassette while said cassette remains a distinct and uncoupled component from said system;

exposing the wafer transport robot to the ambient environment during extension into said cassette;

removing at least one wafer from said cassette;

placing said removed wafer into a load lock chamber via an extendable arm on said robot.

Suda et al. do not teach the cassette as being a FOUP device. Gordon et al. US 6,013,920 teaches a method of handling wafers from a FOUP. It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the methods taught by Suda et al. by providing the cassette as a FOUP as taught by Gordon et al. in order to allow the device to operate using cassettes that maintain the wafers in a clean state as they are moved about the manufacturing area.

In regards to claim 2 Suda et al. also teach that said wafer transport device comprises a robot with an extensible arm and an end effector.

In regards to claim 3 Suda et al. further teach that the wafer transport device is fixed within the transport chamber.

In regards to claim 9 Suda et al. also teaches opening a gate valve assembly between the transport module and the cassette to allow said transport device to extend into said cassette.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda et al. in view of Gordon et al. as applied to claim 1 above, and further in view of Beaulieu et al. (US 5,882,413). Suda et al. in view of Gordon et al. teach the limitation of claim 1 as above they do not teach using a storage location or the type of processing chamber used or the use of a cooling chamber. Beaulieu et al. (US 5,882,413) disclose a method for transporting semiconductor wafers comprising:

providing a processing system (10) including a transport module (12) and a process chamber (14);

extending a semiconductor transport device (22) from said transport module (12) into adjacently positioned container, said container being a separate component from said processing system;

removing at least one wafer (s) from said container using said wafer transporting device;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

placing the wafers (s) in a storage position (34);

wherein the process chamber is a chemical vapor deposition chamber;

transporting the wafers (s) between a cooling chamber (36) and a process chamber (14).

providing a processing system (10) including a transport module (12) and a process chamber (14);

extending a semiconductor transport device (22) from said transport module (12) into adjacently positioned container, said container being a separate component from said processing system;

removing at least one wafer (s) from said container using said wafer transporting device;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

placing the wafers (s) in a storage position (34);

wherein the process chamber is a chemical vapor deposition chamber;

transporting the wafers (s) between a cooling chamber (36) and a process chamber (14).

It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the methods taught by Suda et al. in view of Gordon et al. by moving the wafers into chambers and modules of various sorts are taught by Beaulieu et al. and are well known in the art.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suda et al. in view of Gordon et al. as applied to claim 1 above, and further in view of Moore et al. Suda et al. in view of Gordon et al. teach the limitations of claim 1 as above, they do not teach the processing system as comprising a single rapid thermal processing chamber. Moore et al. (US 6,151,447) teach an apparatus with a rapid thermal processing chamber. It would have been obvious to one of ordinary skill in the art, at the time of invention that a rapid thermal chamber as taught by Moore et al. could have been used as the process chamber taught by Suda et al. in view of Gordon et al. as modular chambers are well know in the art, and said chambers are designed to perform many processing steps including rapid thermal processing.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suda et al. as applied to claim 11 above, and further in view of Beaulieu et al. Suda et al. teach the limitations of claim 11 as above they do not teach the system having a storage

location or the type of processing chamber used or a cooling chamber. Beaulieu et al. disclose an apparatus for transporting semiconductor wafers comprising:

a processing system (10) including a transport module (12) and a process chamber (14);

an extending semiconductor transport device (22) ;

wherein the transport device (22) comprises a robot including an extendible arm and an end effector (29);

and the transport device (22) is in a fixed position;

a storage position (34);

wherein the process chamber is a chemical vapor deposition chamber;

a cooling chamber (36) and a process chamber (14);

It would have been obvious to one of ordinary skill in the art, at the time of invention to modify the device taught by Suda et al. in view of Gordon et al. by providing the chambers and modules of various sorts are taught by Beaulieu et al. as they are well known in the art.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suda et al. as applied to claim 11 above, and further in view of Moore et al. Suda et al. teach the limitations of claim 11 as above, they do not teach the processing system as comprising a single rapid thermal processing chamber. Moore et al. teach an apparatus with a rapid thermal processing chamber. It would have been obvious to one of ordinary skill in the art, at the time of invention that a rapid thermal chamber as taught by Moore et al. could have been used as the process chamber taught by Suda et al. as

modular chambers are well know in the art, and said chambers are designed to perform many processing steps including rapid thermal processing.

Response to Amendment

The amendments to the claims and drawings filed on August 5, 2004 have been entered into the record.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A. Fox whose telephone number is 703-605-4294. The examiner can normally be reached between 7:00-5:00 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eileen D. Lillis can be reached at 703-308-3248. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EILEEN D. LILLIS
SUPERVISORY PATENT EXAMINER
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